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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,187	01/22/2002	Hassan Paddy Abdel Salam	66455-209	9674

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EXAMINER
ROY, SIKHA

ART UNIT	PAPER NUMBER
2879	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,187	SALAM, HASSAN PADDY ABDEL	
	Examiner	Art Unit	
	Sikha Roy	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 38,39 and 40,41and 42,43,45,46,49,52,53-56, 64 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,6 and 7,4, 2, 18, 3, 8, 19, 20-21, 42 respectively of U.S. Patent No. 6,346,771 to Salam.

Regarding claim 38, both instant application and the Patent 6,346,771 in claim 1 claim LED lamp for generating incoherent visible light comprising semiconductor structure having a lower and upper semiconductor layers of opposite conductivities forming a diode and an active region generating light, said semiconductor structure having outer side faces, at least one metal conductor electrically connected with the upper semiconductor layer, a plurality of cavities in the semiconductor structure extending from the upper face, each containing a metal part that is in electrical contact with the lower semiconductor layer and that is distant from the outer side faces,

semiconductor structure having several light-extraction surfaces, LED light propagating in the semiconductor structure being diverted at the light-extraction surfaces and electrical interconnection for causing the metal parts in the cavities to pass current when the lamp is turned on.

Claims 39,40 of the instant application are obvious over claims 6 and 7 of U. S. Patent 6,346,771, both claiming light extraction surfaces being side walls of the cavities or trenches.

Claims 41 and 42 of the instant application are obvious over claim 4 of U. S. Patent 6,346,771, both claiming a metal layer covering most of the top face.

Claim 43 of the instant application is obvious over claim 2 of U. S. Patent 6,346,771, both claiming transparent substrates.

Claim 45 of the instant application is obvious over claim 18 of U. S. Patent 6,346,771, both claiming metal parts in the cavities serve as reflectors.

Claim 46 of the instant application is obvious over claim 3 of U. S. Patent 6,346,771, both claiming light extraction surfaces being oblique to the layer serving as reference plane.

Claim 49 of the instant application is obvious over claim 8 of U. S. Patent 6,346,771, both claiming cavities are cut through the semiconductor structure.

Claim 52 of the instant application obvious over claim 19 of U. S. Patent 6,346,771, both claiming the heat sink less than 50 microns away from the active region.

Claims 53 – 56 of the instant application are obvious over claims 20,21 of U. S. Patent 6,346,771, both claiming LED portions within the semiconductor structure each provided with an associated conductor (metal track) for energizing the portion and an associated electrical link in series with the conductor, some of the LED portions being faulty and having their associated links deliberately disrupted, the disrupted links being disrupted fuses.

Claim 64 of the instant application is obvious over claim 42 of U. S. Patent 6,346,771, both claiming semiconductor structure having first and second LED portions with the cathode of one electrically connected to the anode of the other with a metal conductor.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 67 recites the limitation "LED lamp" in claim 66 but there is no recitation of LED lamp in claim 66. Hence there is insufficient antecedent basis for this limitation in the claim 67.

Claim 69 recites the limitation "LED lamp" in claim 68 but there is no recitation of LED lamp in claim 66. Hence there is insufficient antecedent basis for this limitation in the claim 69.

Claim 85 recites the limitation "said pair of reflective surfaces" in claim 84 while there is no mention of pair of reflective surfaces in claim 84. Hence there is insufficient antecedent basis for this limitation in the claim 85.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 38-52, 56-63, 66-107 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent 5,696,389 to Ishikawa et al. in view of U. S. Patent 6,229,160 to Krames et al.

Ishikawa et al. disclose (column 9 lines 25-40 Fig7) an LED lamp comprising a surface-surrounded semiconductor structure having a lower semiconductor layer 122 having a lower face and an upper semiconductor layer 124 forming a diode and an active region123 between the two layers generating light and a plane parallel to the lower face defining reference plane. Light generated by recombination of holes and electrons pass vertically outside the lamp. There is one metal conductor 126 provided on the cladding layer 124 and electrically connected to the upper layer 124. Ishikawa et al. further disclose the LED lamp comprising of plurality of cavities extending from the

upper face into the semiconductor structure, each containing a metal part 125 that is in electrical contact with the lower semiconductor layer and that is distant from outer faces and passes current when the lamp is turned on. The annular exposed surface of the lower semiconductor layer 122 and upper layer 124 constitute the light radiating surface.

Referring to claim 38 Ishikawa et al. do not exemplify several light extraction surfaces inclined to the reference plane.

Krames et al. in analogous art of semiconductor light-emitting device disclose (abstract) the side surfaces of the cavities are formed at preferred angle relative to the normal to the plane of the light-emitting active layer to improve the light extraction efficiency and increase the total light output efficiency.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify the straight sides of the cavities of the LED lamp of Ishikawa et al. by inclined sides as taught by Krames et al. for improving the light extraction efficiency and hence increasing the total light output efficiency.

Referring to claims 39 and 40 Ishikawa and Krames disclose the sidewalls of the cavities or trenches form the light-extraction surfaces.

Regarding claims 41 and 42 Ishikawa et al. disclose (column 10 lines 27-33) an ohmic contact layer 129, a metal layer, in electrical contact with the upper semiconductor layer resulting in decrease in voltage drop between the two electrodes.

Regarding claim 43 Ishikawa et al. disclose (column 8 lines 23-26) the substrate over which the semiconductor layers are grown is transparent to the light emitted.

Regarding claim 44 Ishikawa et al. disclose (column 21 line 41) the conductor being thin is light-passing.

Regarding claim 45 Ishikawa et al. disclose (column 24 lines52-54) the metal part (electrode 405 in Fig.29) inside the cavity act as reflector for light generated by the active region.

Regarding claim 46 Krames et al. teach the light extraction surfaces are oblique to the reference plane of upper or lower semiconductor layers.

Referring to claim 47 Ishikawa and Krames disclose the upper faces are separated by the sides of the cavities and hence are islands defined by the periphery of the light extraction surfaces.

Referring to claim 48 Ishikawa et al. disclose (column 24 line 43) the LED being resin-molded and hence having amorphous material at the light-extraction surfaces.

Regarding claims 49 and 50 Ishikawa et al. disclose the cavities are inside the semiconductor structure and the light extraction surface (side surface of the cavity) meets the upper face at an angle of 90 degrees.

Regarding claim 51 Ishikawa and Krames disclose the claimed invention except for the meandering conductors. It would have been obvious matter of design choice to have the conductors meandering since the applicant has not disclosed that meandering conductors solves any stated problem and it appears that the invention would perform equally well with the conductors as disclosed by Ishikawa et al.

Referring to claim 52 Krames et al. disclose (column 5 lines 30-34) heat-sink at the bottom window. Krames disclose the claimed invention except for the limitation of

the heat sink within 50 microns of the active region. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 205 USPQ 215 (CCPA 1980). Thus, it would have been obvious to one of ordinary skills in the art at the time the invention was made to specify the distance of the heat sink from the active region to be 50 microns, since discovering an optimum value of a result variable is considered within the skills of the art.

Claim 56 essentially recites the same limitations as of claims 38 and 51.

It is elementary that mere recitation of a newly discovered function or property, intrinsically possessed by things in the prior art, does not cause a claim drawn to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an intrinsic characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. *In re Swinehart*, 169 USPQ 226 (CCPA 1971). Thus, the functional limitation of the active region generating light a substantial proportion of which propagates parallel to the active region is taught by Ishikawa and Krames under intrinsic functional principles. Light produced in the active region includes a part which propagates vertically to the semiconductor layers and is output vertically and a part which propagates parallel to the active region and undergoes multiple internal reflections and is output through the light-extraction

surfaces (side surfaces of the cavities) (as evidenced by U. S. Patent 5,753,940 to Komoto).

Regarding claim 57 Ishikawa et al. disclose the track (metal electrode) on the lower semiconductor.

Claim 58 recites the same limitation as of claim 48 and is rejected for the same reason.

Regarding claim 59, Ishikawa and Krames disclose the claimed invention except for the limitation of the upper face within 10 microns of the lower face. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 205 USPQ 215 (CCPA 1980). Thus, it would have been obvious to one of ordinary skills in the art at the time the invention was made to specify the distance of 10 microns by which the upper face is within the lower face, since discovering an optimum value of a result variable is considered within the skills of the art.

Regarding claim 60 Ishikawa et al. disclose (column 9 lines 60-64, column 10 lines 22-26 Fig.7) a Bragg reflector layer 127 translucent to visible light below the lower semiconductor layer 122 acting as a reflector for the guided light, the semiconductor substrate having higher refractive index than this reflector layer. Light beams traveling toward the substrate are reflected by the Bragg reflection layer 127 and hence more light is emitted from the surface. Ishikawa also discloses opaque conductors 129 on the semiconductor structure appearing between the light generating portions as viewed normal to the reference plane.

Claim 61 recites the same limitation as of claim 44 and hence is rejected for the same reason.

Claim 62 recites the same limitation as of claim 48 and hence is rejected for the same reason.

Claim 63 recites the same limitation as of claim 39 and hence is rejected for the same reason.

Claim 66 essentially recites the same limitation as of claim 38 and the limitation of second conductor (top electrode) crossing over the first conductor (bottom electrode) and being insulated by dielectric material such as resin mold is disclosed by Ishikawa and Krames.

Claim 67 essentially recites the same limitations as of claim 41 and hence is rejected for the same reason.

Regarding claim 68 Ishikawa and Krames disclose the claimed invention except for the limitation that the conductors in electrical contact lower semiconductor layers being U-shaped. It has been held that a change in shape is generally recognized as being within the level of ordinary skill in the art. *In re Dailey*, 357 F.2d 669,149 USPQ 47 (CCPA 1966). It would have been obvious to one having ordinary skill in the art to have the U-shaped conductors, since such a modification would have involve a mere change in the shape of a component.

Claim 69 essentially recites the same limitations as of claim 41 and hence is rejected for the same reason.

Referring to claim 70 Krames et al. disclose (column 5 lines 30-32, Fig.2) a window at the bottom of the surface which radiates heat generated inside the device thus acting as heat sink. It would be obvious to switch the position of the heat sink from the bottom to the top of the upper face since changing the position of an element of the structure is within the skill of the art. Furthermore the applicant has also disclosed (Fig.1 reflective bowl 3 acting as heat sink) one embodiment in which the heat sink is at the bottom of the device indicating it works as well as when it is above the upper surface of the semiconductor layer.

Krames et al. also disclose (column 8 lines 51-55) the semiconductor structure having several light diverting surfaces coated with highly reflective film to inhibit light from escaping out the side-surfaces and promote light exiting through the top surface.

Regarding claim 71 Ishikawa et al. disclose (column 24 lines 52,53) the LED with reflector above the upper face of the semiconductor layer for reflecting back light in the active region.

Regarding claim 72 it is well known in the art to include a dielectric layer under a metallic electrode for preventing short-circuiting.

Claim 73 recites the same limitation as of claim 59 and hence is rejected for the same reason (see rejection of claim 59).

Regarding claim 74 Ishikawa et al. disclose (column 9 lines 27-35, Fig. 7) that the upper semiconductor layer (p-type cladding layer) 124 is grown over the lower semiconductor layer (n-type cladding layer) 122.

Regarding claim 75 Ishikawa and Krames disclose all the limitations which are same as claim 38. Ishikawa discloses opaque conductor in electrical contact with the upper semiconductor layer. It would be obvious to one of ordinary skill in the art to modify the conductor to a plurality of conductors in case of a structure with plurality of light extraction grooves (cavities)and electrical connection made via the conductors when the light is turned on.

Claim 76 essentially recites the same limitation of reflector below the lower face as in claim 60 and hence is rejected for the same reason.

Claims 77,78, 81 essentially recite the same limitation as of claim 75 and hence are rejected for the same reason.

Claim 79 recites the same limitation as of claim 44 and hence is rejected for the same reason.

Regarding claim 80 Ishikawa discloses light-passing substrate and a reflector layer between the substrate and the lower face of the semiconductor layer for redirecting light. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the reflector layer under the substrate since it has been held that rearranging parts of an invention involves only routine skill in the art.

Regarding claim 82 Krames et al. disclose (column 9 lines 46-48, claim 5) the top device area can be a triangle resulted from trenches forming triangular area in the upper face.

Claim 83 recites the same limitation as of claim 44 and hence is rejected for the same reason.

Claim 84 recites the same limitations as of claims of 70 and 71 and hence is rejected for the same reason (see rejection of claims 70,71).

Regarding claims 85 and 88 Krames et al. disclose (column 4 lines 45-60, column 8 lines 51-55) the two side walls forming light diverting-surfaces, coated with reflective films are separated by a space devoid of semiconductor (cavity).

Claim 86 recites the same limitation as of claim 72 and is rejected for the same reason.

Regarding claim 87 Krames discloses the heat sink at the bottom window. Ishikawa and Krames disclose the claimed invention except for the metallic reflectors providing the heat sink. It would have been obvious matter of design choice to have the heat sink at the top of the upper conductor layer provided by the metallic reflector since the applicant has not disclosed that this design of heat sink solves any stated problem and it appears that the invention would perform equally well with the heat sink as disclosed by Ishikawa and Krames et al.

Regarding claim 89 Ishikawa et al. disclose the upper face covered with a conductor layer in electrical contact with the upper semiconductor layer.

Claim 90 recites the same limitation as of claim 47 and is rejected for the same reason.

Claim 91 recites the same limitation as of claim 49 and is rejected for the same reason.

Regarding claim 92 Ishikawa and Krames disclose all the limitations which are same as of claim 38 and hence is rejected for the same reason.

Claims 93,94 and 95 recite the limitations same as of claims 49,42 and 44 respectively and hence are rejected for the same reasons (see rejection of claims 49,42 and 44).

Claims 96 and 97 recite the same limitations as of claims 60 and 46 respectively and hence are rejected for the same reasons.

Regarding claims 98 and 99 Ishikawa et al. disclose the substrate made of sapphire on which the semiconductor structure is grown.

Claim 100 recites the limitations same as of claim 38 and 56 and hence is rejected for the same reasons (see rejection of claims 38 and 56).

Claim 101 recites the same limitation as of claim 46 and hence is rejected for the same reason.

Regarding claim 102 the side walls of plurality of cavities form the sides of separate LEDs as evidenced by U. S. Patent 3,900,863 to Kim.

Referring to claim 103 Ishikawa et al. disclose (Fig. 8 fourth embodiment) lower semiconductor layer (n-type cladding layer)134 comprises a sublayer of low resistivity.

Regarding claim 104 Krames et al. disclose (column 4 lines 54-67) that the side-walls pass light.

Claim 105 recites the same limitation of crossing of second conductor over the first conductor and insulation preventing electrical contact between the two as in claim 66 and is rejected for the same reason.

Claim 106 recites the same limitation as of claim 38 and hence is rejected for the same reason.

Claim 107 recites the same limitation as of claim 60 and hence is rejected for the same reason.

Claims 64,65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent 5,696,389 to Ishikawa et al. and U. S. Patent 6,229,160 to Krames et al. and further in view of U. S. Patent 4,225,380 to Wickens.

Claim 64 differs from Ishikawa and Krames in that Ishikawa and Krames do not exemplify semiconductor structure comprising array of LED portions and electrical connections for energizing several LED portions.

Wickens in analogous art of producing light emitting semiconductor display disclose (abstract, Figs. 3 and 5) LED lamp comprising light-emitting semiconductor devices formed in a silicon wafer substrate and electrical connection for energizing the array.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to specify the electrical connection of the cathode and anode of the LED device of Ishikawa and Krames as taught by Wickens for forming and energizing an array of LED portions.

Referring to claim 65 Wickens discloses (Fig.5 column 4 lines 56-65) first and second set of LED portions connected in parallel.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art references are cited to further show the state of the art with respect to semiconductor light-emitting devices.

U. S. Patent 4,881,237 to Donnelly.

U. S. Patent 5,113,232 to Itoh et al.

U. S. Patent 5,905,275 to Nunoue et al.

U. S. Patent 5,753,940 to Komoto.

U. S. Patent 6,015,719 to Kish et al.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (703) 308-2826. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (703) 305-4794. The fax phone number for the organization is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

S.R.

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